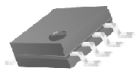
FEATURES

- Guaranteed 3A Output Current
- Efficiency up to 94%
- Efficiency up to 80% at Light Load (10mA)
- Operate from 2.8V to 5.5V Supply
- Adjustable Output from 0.8V to VIN*0.9
- Internal Soft-Start
- Short-Circuit and Thermal -Overload Protection
- 1MHz Switching Frequency Reduces Component size

SOP8-PP PKG



ORDERING INFORMATION

Device	Package
TJ6813DP	SOP8-PP

APPLICATION

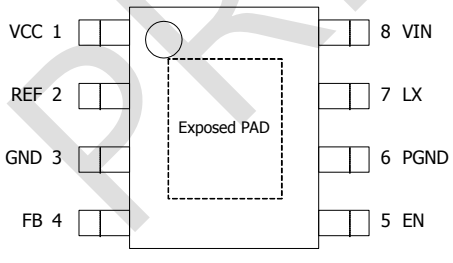
- ASIC/DSP/µP/FPGA Core and I/O Voltages
- Set-Top Boxes
- Networking and Telecommunications
- Cellular Base Stations
- Servers
- TVs

DESCRIPSION

The TJ6813 high-efficiency, DC-DC step-down switching regulator delivers up to 3A of output current The device operates from an input voltage range of 2.8V to 5.5V and provides an adjustable output voltage from 0.8V to VIN*0.9, making the TJ6813 ideal for on-board post regulation applications. The efficiency of TJ6813 at light load (10mA) is up to 80%, and efficiency at heavy load is up to 94%.

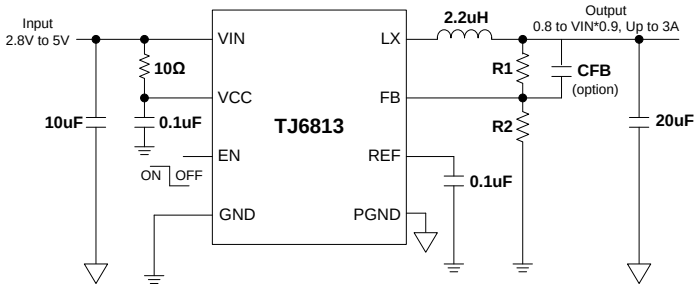
The TJ6813 operates at a fixed frequency of 1MHz. The high operating frequency minimizes the size of external components. Internal soft-start circuitry reduces inrush current. Short-circuit and thermal-overload protections improve design reliability.

PIN CONFIGURATION



SOP8-PP

Typical Application Circuit



$$V_{OUT} = 0.8V \cdot \left(1 + \frac{R1}{R2}\right)$$

Absolute Maximum Ratings

SYMBOL	MIN.	MAX.	UNIT	SYMBOL	MIN.	MAX.	UNIT
VIN, VCC, REF to GND	-0.3	6.5	V	Operating Temp. Range	-40	125	℃
EN, FB to GND	-0.3	VCC+0.3	V	Junction Temp. Range	-40	125	℃
PGND to GND	-0.3	0.3	V	Storage Temp. Range	-65	150	℃
LX current	-3.5	3.5	A	Lead Temperature (Soldering, 5s)		260	℃

(1) It is recommended for V_{EN} not to exceed V_{IN} Voltage

ELECTRICAL CHARACTERISTICS(Note 1)

Limits in standard typeface are for TJ=25℃. VIN=VCC=5V, PGND=GND, FB in regulation, CREF=100nF, TA=-40°C to +125°C, unless otherwise noted. Typical values are at TA=+25°C.

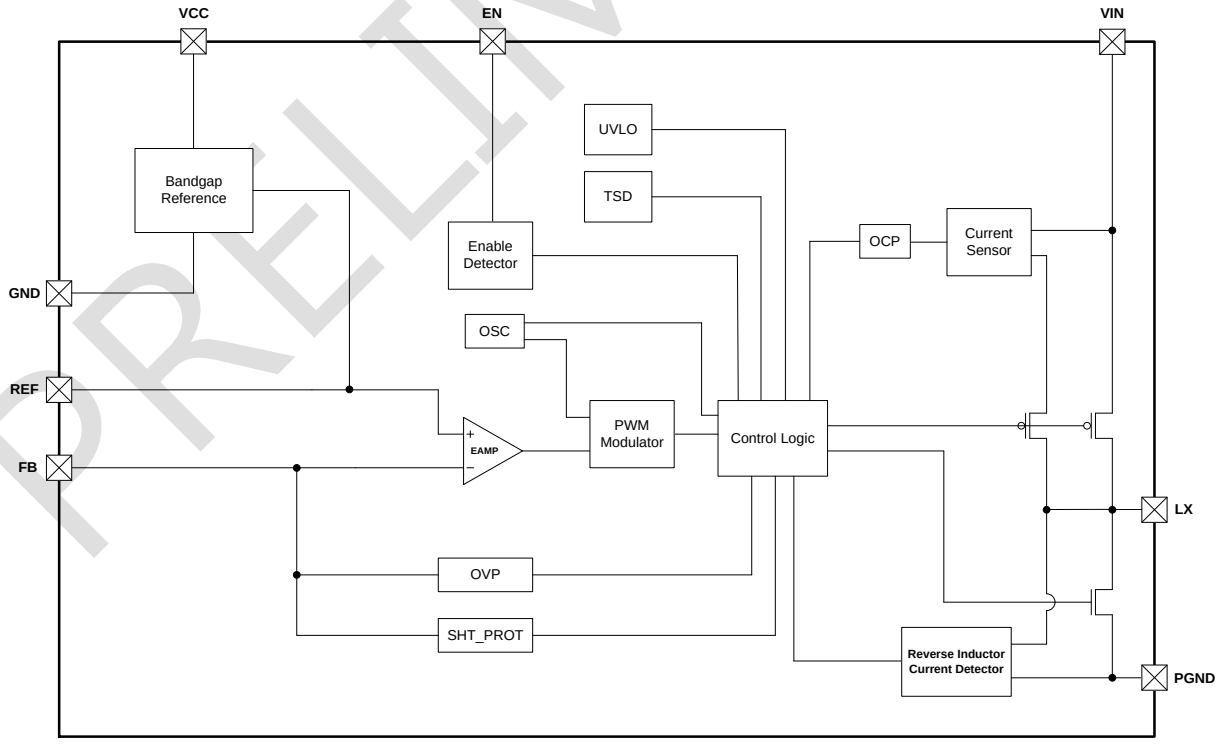
PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage Range			2.8		5.5	V
Supply Current	Switching with no load, LX floating	VIN=5.0V		1	2	mA
Shutdown Current	EN=GND			1	5	uA
VCC Undervoltage Lockout Threshold	When LX starts/stops switching	VCC Rising		2.7		V
		VCC Falling		2.6		
REF Voltage	IREF=0, VIN=2.8V to 5V			0.8		
Output Voltage Range	when using external feedback resistors to drive FB		0.8		VIN*0.9	V
Output Voltage Line Regulation	VIN = 3V to 5V			0.5		%/V
Output Voltage Load Regulation	ILOAD = 0A to 3A			0.5		%/A
FB Regulation Voltage	ILOAD = 0A to 1.5A, VIN = 2.8V to 5.0V		- 0.776	0.8 -	- 0.824	V
FB Input Bias Current			-0.1		0.1	uA
LX On-Resistance, PMOS	VIN = 5V			100		mΩ
LX On-Resistance, NMOS	VIN = 5V			90		mΩ
LX Current-Limit Threshold	Duty cycle = 90%, VIN=2.8V to 5.0V	High side	4.1	4.8		A
		Low side		0		A
LX Leakage Current	VIN=5.0V	VLX=5.0V			10	uA
		VLX=GND	-10			uA
LX Switching Frequency	VIN = 2.8V to 5.0V		-	1	-	MHz
LX Maximum Duty Cycle	VFB=GND, LX=High-Z, VIN=2.8V to 5.0V		90			%
LX Minimum Duty Cycle	VFB=VIN, VIN=2.8V to 5.0V			10		%
Output Variation by Temperature	Temp = 25 to 160			3		%
Thermal-Shutdown Threshold 1)	When LX starts/stops switching	TJ rising		160		°C
		TJ falling		145		°C
EN Enable Threshold	Logic High		1.7			V
	Logic Low				1.3	V

Note 1). Guaranteed by design, Not tested

PIN DESCRIPTION

PIN	Name	Function
1	VCC	Analog Supply Voltage. Bypass with 0.1uF capacitor to ground and 10Ω resistor to VIN
2	REF	Reference Bypass. Bypass with 100nF capacitor to ground.
3	GND	Analog ground
4	FB	Feedback input. Connect an external resistor-divider from the output to FB and GND to set the output to a voltage between 0.8V and VIN*0.9
5	EN	Enable. (Enable : EN=VCC, Disable : EN=GND)
6	PGND	Power Ground. Keep power ground and analog ground planes separate.
7	LX	Inductor Connection. Connect an inductor between LX and the regulator output.
8	VIN	Power-supply voltage. Input voltage range from 2.8V to 5.0V. Bypass with a 10uF(min.) ceramic capacitor to ground and a 10Ω resistor to VCC
-	Exposed Thermal PAD	Connect to ground

Block Diagram



TYPICAL OPERATING CHARACTERISTICS

T.B.D

TYPICAL OPERATING CHARACTERISTICS

T.B.D

Detailed Description

The TJ6813 high-efficiency switching regulator is a small, simple, internal compensation, voltage-mode DC-DC step-down converter capable of delivering up to 3A of output current. The device operates in pulse-width modulation (PWM) at a fixed frequency of 1MHz from a 2.8V to 5.0V input voltage and provides an output voltage from 0.8V to VIN*0.9, making the TJ6813 ideal for on-board post regulation applications. The high switching frequency allows for the use of smaller external components, and an internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on-resistance of the internal high-side MOSFET to sense switching currents eliminates current sense resistors, further improving efficiency and cost.

Controller Block Function

The TJ6813 step-down converter uses a PWM voltage-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against ramp signal. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The voltage mode feedback system regulates the peak inductor current as a function of the output-voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (< 30% ripple current), the circuit acts as a switch-mode transconductance amplifier. During the second half of the cycle, the internal high-side p-channel MOSFET turns off, and the internal low-side n-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current, and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit (see the Current Limit section), the high-side MOSFET does not turn on at the rising edge of the clock and the low-side MOSFET remains on to let the inductor current ramp down.

Current Sense

An internal current-sense amplifier produces a current signal proportional to the voltage generated by the high-side MOSFET on-resistance and the inductor current (RDS(ON) x ILX). The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the output from the voltage-error amplifier.

Current Limit

The internal high-side MOSFET has a current limit of 4.8A (typ). If the current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. This lowers the duty cycle and causes the output voltage to drop until the current limit is no longer exceeded. A synchronous rectifier current limit of 0A (typ) protects the device from current flowing into LX. If the negative current limit is exceeded, the synchronous rectifier turns off, forcing the inductor current to flow through the high-side MOSFET body diode, back to the input, until the beginning of the next cycle or until the inductor current drops to zero. The TJ6813 utilizes a pulse-skip mode to prevent overheating during short-circuit output conditions. The device enters pulse-skip mode when the FB voltage drops below 300mV, limiting the current to 4.8A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

VCC Decoupling

Due to the high switching frequency , decouple VCC with a 1μF capacitor connected from VCC to GND, and a 10Ω resistor connected from VCC to IN. Place the capacitor as close as possible to VCC.

Soft Start

The TJ6813 employs internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under voltage lockout (UVLO) shutdown mode, or restarts following a thermal-overload event, or EN is driven high, the digital soft-start circuitry slowly ramps up the voltage to the error-amplifier noninverting input.

Undervoltage Lockout

If VCC drops below 2.6V, the UVLO circuit inhibits switching. Once VCC rises above 2.7V, the UVLO clear and the soft-start sequence activates.

Shutdown Mode

Use the enable input, EN, to turn on or off the TJ6813. Connect EN to VCC for normal operation. Connect EN to GND to place the device in shutdown. Shutdown causes the internal switches to stop switching and forces LX into a high-impedance state. In shutdown, the TJ6813 draws under 1μA of supply current. The device initiates a soft-start sequence when brought out of shutdown.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ = +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Application Information

Adjustable Output Voltage

The TJ6813 provides an adjustable output voltage between 0.8V and VIN*0.9. Connect FB to output for 0.8V output. To set the output voltage of the TJ6813 to a voltage greater than VFB (0.8V typ), connect the output to FB and GND using a resistive divider, as shown in Typical Application Circuit. Choose R2 between 2kΩ and 20kΩ, and set R1 according to the following equation:

R1 = R2 x [(VOUT/VFB) - 1]

The TJ6813 PWM circuitry is capable of a stable minimum duty cycle of 30%. This limits the minimum output voltage that can be generated to 0.30*VIN with an absolute minimum of 0.8V. Instability may result for VOUT/VIN ratios below 0.30.

Output Inductor Selection

Use a 2μH inductor with a minimum 3A-rated DC current for most applications. For best efficiency, use an inductor with a DC resistance of less than 20mΩ and a saturation current greater than 5A (min). For most designs, derive a reasonable inductor value (L_{INIT}) from the following equation:

L_{INIT} = VOUT x (VIN - VOUT)/(VIN x LIR x IOUT(MAX) x f_{SW})

where f_{SW} is the switching frequency (1MHz typ) of the oscillator. Keep the inductor current ripple percentage LIR between 20% and 40% of the maximum load current for the best compromise of cost, size, and performance. Calculate the maximum inductor current as:

IL(MAX) = (1 + LIR/2) x IOUT(MAX)

Check the final values of the inductor with the output ripple voltage requirement. The output ripple voltage is given by:

VRIPPLE = VOUT x (VIN - VOUT) x ESR/(VIN x LFINAL x f_{SW})

where ESR is the equivalent series resistance of the output capacitors.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = (1/VIN) \times \sqrt{(I_{OUT}{}^2 \times V_{OUT} \times (V_{IN} - V_{OUT}))}$$

For duty ratios less than 0.5, the input capacitor RMS current is higher than the calculated current. Therefore, use a +20% margin when calculating the RMS current at lower duty cycles. Use ceramic capacitors for their low ESR and equivalent series inductance (ESL). Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability. After determining the input capacitor, check the input ripple voltage due to capacitor discharge when the high-side MOSFET turns on. Calculate the input ripple voltage as follows:

VIN_RIPPLE = (IOUT x VOUT)/(f_{SW} x VIN x CIN)

Keep the input ripple voltage less than 3% of the input voltage.

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and the voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

VRIPPLE = VRIPPLE(C) + VRIPPLE(ESR) + VRIPPLE(ESL)

where the output ripple due to output capacitance, ESR, and ESL is:

$V_{RIPPLE(C)} = I_{P-P}/(8 \times C_{OUT} \times f_{SW})$

$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$

$V_{RIPPLE(ESL)} = (I_{P-P}/tON) \times ESL$ or $(I_{P-P}/tOFF) \times ESL$,

whichever is greater and I_{P-P} the peak-to-peak inductor current is:

$I_{P-P} = [(V_{IN} - V_{OUT})/f_{SW} \times L)] \times V_{OUT}/V_{IN}$

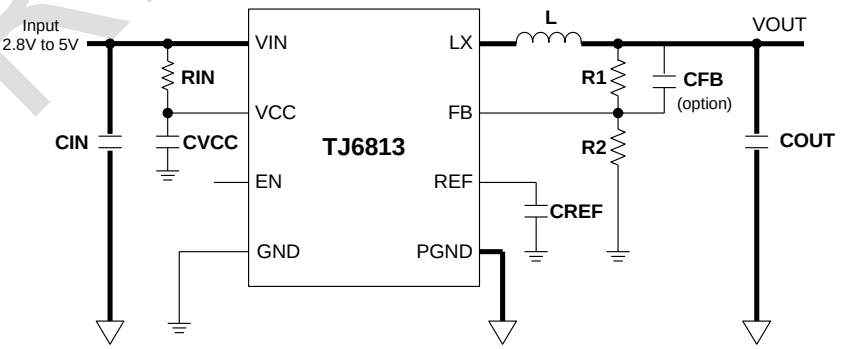
Use these equations for initial capacitor selection, but determine final values by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for their low ESR and ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible. Load-transient response depends on the selected output capacitor. During a load transient, the output instantly changes by ESR x ΔILOAD. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the Load Transient graph in the Typical Operating Characteristics), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, thus preventing the output from deviating further from its regulating value.

PCB Layout Considerations

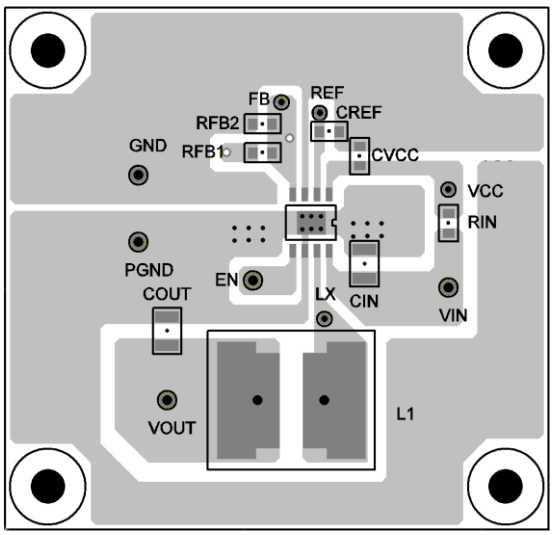
Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close as possible to the IC. Keep the power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (CIN to IN and CIN to PGND) short. Avoid vias in the switching paths.
4) If possible, connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close as possible to the IC.
6) Route high-speed switching nodes away from sensitive analog areas (FB).

EVB Schematic



Top Layout



Bottom Layer